EAST Search History

Ref	Hits	Search Query	DBs	Default	Plurals	Time Stamp
#				Operator		
L1	1067538	active or inactive or standby	US-PGPUB; USPAT	OR	ON	2006/03/01 10:06
L2	48701	sram	US-PGPUB; USPAT	OR	ON	2006/03/01 10:06
L3	23683	1 and 2	US-PGPUB; USPAT	OR	ON	2006/03/01 10:06
L4	2035	365/226.ccls.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:26
L5	340	3 and 4	US-PGPUB; USPAT	OR	ON	2006/03/01 10:06
L6	914	365/227.ccls.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:06
L7	234	3 and 6	US-PGPUB; USPAT	OR	ON	2006/03/01 10:08
L8	1337	body adj bias	US-PGPUB; USPAT	OR	ON	2006/03/01 10:09
L9	1	7 and 8	US-PGPUB; USPAT	OR	ON	2006/03/01 10:08
L10	3187	back adj bias	US-PGPUB; USPAT	OR	ON	2006/03/01 10:09
L11	7	7 and 10	US-PGPUB; USPAT	OR	ON	2006/03/01 10:11
L12	4466	8 or 10	US-PGPUB; USPAT	OR	ON	2006/03/01 10:11
L13	25	5 and 12	US-PGPUB; USPAT	OR	ON	2006/03/01 10:11
L14	1887	365/154.ccls.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:27
L15	595	3 and 14	US-PGPUB; USPAT	OR	ON	2006/03/01 10:27
L16	33	12 and 15	US-PGPUB; USPAT	OR	ON	2006/03/01 10:34
L17	30	tang-stephen-h\$.in.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:34
L18	32	khellah-muhammad-m\$.in.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:34
L19	66	somasekhar-dinesh.in.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:35
L20	159	de-vivek-k\$.in.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:35
L21	34	tschanz-james-w\$.in.	US-PGPUB; USPAT	OR	ON	2006/03/01 10:35



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Inventor Name Search Result

Your Search was:

Last Name = TANG

First Name = STEPHEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>10748222</u>	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
10987278	Not Issued	41	11/12/2004	Level shifter	TANG, STEPHEN
11066395	Not Issued	95	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	TANG, STEPHEN
11111060	Not Issued	30	04/21/2005	Level shifter	TANG, STEPHEN
<u>10014009</u>	Not Issued	161	12/10/2001	BALANCING GATE- LEAKAGE CURRENT IN DIFFERENTIAL PAIR CIRCUITS	TANG, STEPHEN H.
10025047	6693332	150	12/19/2001	CURRENT REFERENCE APPARATUS	TANG, STEPHEN H.
10162929	6643199	150	06/04/2002	MEMORY WITH REDUCED SUB-THRESHOLD LEAKAGE CURRENT IN DYNAMIC BIT LINES OF READ PORTS	TANG, STEPHEN H.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	TANG, STEPHEN H.
10330652	Not Issued	20	12/27/2002	Multi-ported register files	TANG, STEPHEN H.
10334644	6710642	150	12/30/2002	BIAS GENERATION CIRCUIT	TANG, STEPHEN H.
10673283	Not Issued	161		Local bias generator for adaptive forward body bias	TANG, STEPHEN H.
10689128	6975005	150		CURRENT REFERENCE APPARATUS AND SYSTEMS	TANG, STEPHEN H.

10716755	Not Issued	71	11/19/2003	Floating-body dram with two- phase write	TANG, STEPHEN H.
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	TANG, STEPHEN H.
10738216	Not Issued	95	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TANG, STEPHEN H.
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	TANG, STEPHEN H.
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	TANG, STEPHEN H.
10747084	6870418	150	12/30/2003	TEMPERATURE AND/OR PROCESS INDEPENDENT CURRENT GENERATION CIRCUIT	TANG, STEPHEN H.
10749734	Not Issued	41	12/30/2003	1P1N 2T gain cell	TANG, STEPHEN H.
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	TANG, STEPHEN H.
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	TANG, STEPHEN H.
10812894	Not Issued	71	03/31/2004	SRAM device having forward body bias control	TANG, STEPHEN H.
10879480	Not Issued	77		Floating-body dynamic random access memory and method of fabrication in tri-gate technology	TANG, STEPHEN H.
<u>10879486</u>	Not Issued	20	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TANG, STEPHEN H.
10880337	Not Issued	41	06/29/2004	Overvoltage detection apparatus, method, and system	TANG, STEPHEN H.
10881001	Not Issued	30	06/30/2004	Two transistor gain cell, method, and system	TANG, STEPHEN H.
10942019	Not Issued	30	09/16/2004	Charge storage memory cell	TANG, STEPHEN H.
10953865	Not Issued	30	09/30/2004	System and method for applying within-die adaptive body bias	TANG, STEPHEN H.
10954537	Not Issued	30	09/29/2004	Crosspoint memory array utilizing one time programmable antifuse cells	TANG, STEPHEN H.

10954931	Not Issued	30	09/30/2004	Floating-body memory cell write	TANG, STEPHEN H.
10956195	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	TANG, STEPHEN H.
10956285	Not Issued	30	09/30/2004	Non volatile data storage through dielectric breakdown	TANG, STEPHEN H.
<u>10956407</u>	Not Issued	93	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	TANG, STEPHEN H.
10979605	Not Issued	30	11/01/2004	OTP antifuse cell and cell array	TANG, STEPHEN H.
10982266	Not Issued	30	11/03/2004	Processor apparatus with body bias circuitry to delay thermal throttling	TANG, STEPHEN H.
11008666	Not Issued	30	02/22/2005	2-Transistor floating-body dram	TANG, STEPHEN H.
11027476	Not Issued	30	12/28/2004	One time programmable memory	TANG, STEPHEN H.
11038134	Not Issued	30	01/21/2005	Bias generator for body bias	TANG, STEPHEN H.
11038394	Not Issued	30	01/21/2005	Bias generator for body bias	TANG, STEPHEN H.
<u>11053786</u>	Not Issued	30	02/09/2005	Non strobe sensing circuit	TANG, STEPHEN H.
11134450	Not Issued	30	05/23/2005	Reducing power consumption in integrated circuits	TANG, STEPHEN H.
11151982	Not Issued	30	11	Purge-based floating body memory	TANG, STEPHEN H.
11158518	Not Issued	30	06/21/2005	Apparatus and method for programming a memory array	TANG, STEPHEN H.
11170504	Not Issued	30	06/29/2005	Capacitor structure for a logic process	TANG, STEPHEN H.
11239903	Not Issued	30	09/30/2005	Dual gate oxide one time programmable (OTP) antifuse cell	TANG, STEPHEN H.
11268098	Not Issued	30	11/07/2005	Asymmetric memory cell	TANG, STEPHEN H.
11268430	Not Issued	30	11/07/2005	Memory cell without halo implant	TANG, STEPHEN H.
11289621	Not Issued	30	11/30/2005	Floating-body dynamic random access memory with purge line	TANG, STEPHEN H.
11295400	Not Issued	20	12/06/2005	Component reliability budgeting system	TANG, STEPHEN H.

11320789	Not Issued			Method and apparatus to clamp SRAM supply voltage	TANG, STEPHEN H.				
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***************************************]	Last Name	First Name					
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Day: Wednesday

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Inventor Name Search Result

Your Search was:

Last Name = KHELLAH
First Name = MUHAMMAD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	KHELLAH, MUHAMMAD
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	KHELLAH, MUHAMMAD
11066395	Not Issued	95	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	KHELLAH, MUHAMMAD
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	KHELLAH, MUHAMMAD M.
10305753	6909652	150	11/26/2002	SRAM BIT-LINE REDUCTION	KHELLAH, MUHAMMAD M.
10330652	Not Issued	20	12/27/2002	Multi-ported register files	KHELLAH, MUHAMMAD M.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	KHELLAH, MUHAMMAD M.
10334456	6831871	150	12/30/2002	STABLE MEMORY CELL READ	KHELLAH, MUHAMMAD M.
10334746	Not Issued	30		Method and apparatus for bus repeater tapering	KHELLAH, MUHAMMAD M.
10716755	Not Issued	71	11/19/2003	Floating-body dram with two- phase write	KHELLAH, MUHAMMAD M.
<u>10721184</u>	7002842	150		FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY	

<u> </u>	<u> </u> ·			WITH PURGE LINE	l i
10738216	Not Issued	95	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	KHELLAH, MUHAMMAD M.
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
<u>10740551</u>	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	KHELLAH, MUHAMMAD M.
10746148	6906973	150	II I	BITE-LINE DROOP REDUCTION	KHELLAH, MUHAMMAD M.
10749734	Not Issued	41	12/30/2003	1P1N 2T gain cell	KHELLAH, MUHAMMAD M.
10750572	6992339	150	II I	ASYMMETRIC MEMORY CELL	KHELLAH, MUHAMMAD M.
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	KHELLAH, MUHAMMAD M.
10812894	Not Issued	71		SRAM device having forward body bias control	KHELLAH, MUHAMMAD M.
10813084	6992603.	150	03/31/2004	SINGLE-STAGE AND MULTI- STAGE LOW POWER INTERCONNECT ARCHITECTURES	KHELLAH, MUHAMMAD M.
10879480	Not Issued	77	06/30/2004		KHELLAH, MUHAMMAD M.
10880337	Not Issued	41		Overvoltage detection apparatus, method, and system	KHELLAH, MUHAMMAD M.
10880988	Not Issued	71	06/30/2004	Interconnect structure in integrated circuits	KHELLAH, MUHAMMAD M.
10881001	Not Issued	30	06/30/2004	Two transistor gain cell, method, and system	KHELLAH, MUHAMMAD M.
10942019	Not Issued	30	09/16/2004	Charge storage memory cell	KHELLAH, MUHAMMAD M.
10947765	Not Issued	30	09/23/2004	Majority voter apparatus, systems, and methods	KHELLAH, MUHAMMAD M.
10954537	Not Issued	30	09/29/2004	Crosspoint memory array utilizing one time programmable antifuse cells	KHELLAH, MUHAMMAD M.

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<u>10954931</u>	Not Issued	30	09/30/2004	Floating-body memory cell write	KHELLAH, MUHAMMAD M.
10956195	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	KHELLAH, MUHAMMAD M.
10956285	Not Issued	30	09/30/2004	Non volatile data storage through dielectric breakdown	KHELLAH, MUHAMMAD M.
10956407	Not Issued	93	09/30/2004	APPARATUS AND METHOD FOR A ONE-PHASE WRITE TO A ONE-TRANSISTOR MEMORY CELL ARRAY	KHELLAH, MUHAMMAD M.
10979605	Not Issued	30	11/01/2004	OTP antifuse cell and cell array	KHELLAH, MUHAMMAD M.
11001870	Not Issued	30	12/01/2004	Memory circuit	KHELLAH, MUHAMMAD M.
11008666	Not Issued	30	02/22/2005	2-Transistor floating-body dram	KHELLAH, MUHAMMAD M.
11027476	Not Issued	30	12/28/2004	One time programmable memory	KHELLAH, MUHAMMAD M.
11053786	Not Issued	30	02/09/2005	Non strobe sensing circuit	KHELLAH, MUHAMMAD M.
11053788	Not Issued	30	02/09/2005	Majority voter circuit design	KHELLAH, MUHAMMAD M.
11059174	Not Issued	20		Representative majority voter for bus invert coding	KHELLAH, MUHAMMAD M.
11134450	Not Issued	30		Reducing power consumption in integrated circuits	KHELLAH, MUHAMMAD M.
11137905	Not Issued	30		Memory with dynamically adjustable supply	KHELLAH, MUHAMMAD M.
11151982	Not Issued	30	06/14/2005	Purge-based floating body memory	KHELLAH, MUHAMMAD M.
11158518	Not Issued	30	06/21/2005	Apparatus and method for programming a memory array	KHELLAH, MUHAMMAD M.
<u>11169106</u>	Not Issued	20	06/27/2005	Memory cell driver circuits	KHELLAH, MUHAMMAD M.
11170504	Not Issued	30	06/29/2005	Capacitor structure for a logic process	KHELLAH, MUHAMMAD M.
11172078	Not Issued	30	06/29/2005	Memory circuit	KHELLAH, MUHAMMAD M.
11172742	Not Issued	30	06/30/2005	Operating an information storage cell array	KHELLAH, MUHAMMAD M.
11225912	Not Issued	20	09/13/2005	Memory cell having p-type pass device	KHELLAH, MUHAMMAD M.
11239903	Not	30	09/30/2005	Dual gate oxide one time	KHELLAH,

	Issued		1 1	programmable (OTP) antifuse cell	MUHAMMAD M.
11268098	Not Issued	30	11/07/2005	Asymmetric memory cell	KHELLAH, MUHAMMAD M.

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Inventor Name Search Result

Your Search was:

Last Name = SOMASEKHAR

First Name = DINESH

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08412183	Not Issued	161		APPARATUS AND METHOD FOR A REDUCED POWER MEMORY DIFFERENTIAL VOLTAGE SENSE- AMPLIFIER	SOMASEKHAR, DINESH
08937832	<u>6014041</u>	150	09/26/1997	DIFFERENTIAL CURRENT SWITCH LOGIC GATE	SOMASEKHAR, DINESH
08997071	6002272	150	12/23/1997		SOMASEKHAR, DINESH
09539933	6421289	150	03/31/2000	METHOD AND APPARATUS FOR CHARGE-TRANSFER PRE-SENSING	SOMASEKHAR, DINESH
09690513	6496402	150	10/17/2000	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
09690687	6421269	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE WITHIN DRAM STORAGE CELLS	SOMASEKHAR, DINESH
09733216	6459316	150	12/08/2000	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
09733482	6701339	150	12/08/2000	PIPELINED COMPRESSOR CIRCUIT	SOMASEKHAR, DINESH
09740104	6351156	150	12/18/2000	Noise reduction circuit	SOMASEKHAR, DINESH
09796072	6982589	150		MULTI-STAGE MULTIPLEXER	SOMASEKHAR, DINESH
09823575	6608786	150			SOMASEKHAR, DINESH
09873557	Not Issued	93		FLOATING POINT MULTIPLY ACCUMULATOR	SOMASEKHAR, DINESH

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09873721	6889241	150	06/04/2001	FLOATING POINT ADDER	SOMASEKHAR, DINESH
09941053	6567329	150	08/28/2001	MULTIPLE WORD-LINE ACCESSING AND · ACCESSOR	SOMASEKHAR, DINESH
09966586	6757784	150	09/28/2001	HIDING REFRESH OF MEMORY AND REFRESH- HIDDEN MEMORY	SOMASEKHAR, DINESH
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	SOMASEKHAR, DINESH
10208130	6597223	150	07/30/2002	FLIP FLOP CIRCUIT	SOMASEKHAR, DINESH
10241791	6707708	150	09/10/2002	STATIC RANDOM ACCESS MEMORY WITH SYMMETRIC LEAKAGE- COMPENSATED BIT LINE	SOMASEKHAR, DINESH
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY BIAS GRID	SOMASEKHAR, DINESH
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	SOMASEKHAR, DINESH
10300398	6721222	150	11/19/2002	NOISE SUPPRESSION FOR OPEN BIT LINE DRAM ARCHITECTURES	SOMASEKHAR, DINESH
10305753	6909652	150		SRAM BIT-LINE REDUCTION	SOMASEKHAR, DINESH
10316728	6707755	150	12/11/2002	HIGH VOLTAGE DRIVER	SOMASEKHAR, DINESH
10324177	6879531	150	12/19/2002	REDUCED READ DELAY FOR SINGLE-ENDED SENSING	SOMASEKHAR, DINESH
10324178	6724649	150	12/19/2002	MEMORY CELL LEAKAGE REDUCTION	SOMASEKHAR, DINESH
10334456	<u>6831871</u>	150	12/30/2002	STABLE MEMORY CELL READ	SOMASEKHAR, DINESH
10461293	6801465	150	06/13/2003	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	SOMASEKHAR, DINESH
10691342	Not	41	10/21/2003	Hiding refresh of memory and	SOMASEKHAR,

	Issued			refresh-hidden memory	DINESH
<u>10716755</u>	Not Issued	71		Floating-body dram with two- phase write	SOMASEKHAR, DINESH
10721178	Not Issued	41	11/26/2003	Systolic memory arrays	SOMASEKHAR, DINESH
10721184	7002842	150	11/26/2003	FLOATING-BODY DYNAMIC RANDOM ACCESS MEMORY WITH PURGE LINE	SOMASEKHAR, DINESH
10738216	Not Issued	95	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	SOMASEKHAR, DINESH
10738220	6876571	150	12/18/2003	STATIC RANDOM ACCESS MEMORY HAVING LEAKAGE REDUCTION CIRCUIT	SOMASEKHAR, DINESH
10740551	6952376	150	12/22/2003	METHOD AND APPARATUS TO GENERATE A REFERENCE VALUE IN A MEMORY ARRAY	SOMASEKHAR, DINESH
10746148	6906973	150	12/24/2003	BITE-LINE DROOP REDUCTION	SOMASEKHAR, DINESH
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	SOMASEKHAR, DINESH
10749734	Not Issued	41	12/30/2003	1P1N 2T gain cell	SOMASEKHAR, DINESH
10750566	7001811	150	12/31/2003	METHOD FOR MAKING MEMORY CELL WITHOUT HALO IMPLANT	SOMASEKHAR, DINESH
10750572	6992339	150	12/31/2003	ASYMMETRIC MEMORY CELL	SOMASEKHAR, DINESH
10810093	6985380	150	03/26/2004	SRAM WITH FORWARD BODY BIASING TO IMPROVE READ CELL STABILITY	SOMASEKHAR, DINESH
10812894	Not Issued	71	03/31/2004	SRAM device having forward body bias control	SOMASEKHAR, DINESH
10879480	Not Issued	77	06/30/2004	Floating-body dynamic random access memory and method of fabrication in tri-gate technology	SOMASEKHAR, DINESH
10880337	Not Issued	41	06/29/2004	Overvoltage detection apparatus, method, and system	SOMASEKHAR, DINESH

<u>10881001</u>	Not Issued	30		Two transistor gain cell, method, and system	SOMASEKHAR, DINESH
10942019	Not Issued	30	09/16/2004	Charge storage memory cell	SOMASEKHAR, DINESH
10947869	Not Issued	41		Gating for dual edge-triggered clocking	SOMASEKHAR, DINESH
10954537	Not Issued	30		Crosspoint memory array utilizing one time programmable antifuse cells	SOMASEKHAR, DINESH
10954931	Not Issued	30	1	Floating-body memory cell write	SOMASEKHAR, DINESH
10956195	Not Issued	93	09/30/2004	SRAM CELL POWER REDUCTION CIRCUIT	SOMASEKHAR, DINESH
10956285	Not Issued	30		Non volatile data storage through dielectric breakdown	SOMASEKHAR, DINESH

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Inventor Name Search Result

Your Search was:

Last Name = DE

First Name = VIVEK

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Application#		=			Inventor Name
<u>08997071</u>	6002272	150	12/23/1997	TRI-RAIL DOMINO CIRCUIT	DE, VIVEK
09001449	5986473	150	12/31/1997	DIFFERENTIAL, MIXED SWING, TRISTATE DRIVER CIRCUIT FOR HIGH PERFORMANCE AND LOW POWER ON-CHIP INTERCONNECTS	DE, VIVEK
10117163	6724648	150	04/05/2002	SRAM ARRAY WITH DYNAMIC VOLTAGE FOR REDUCING ACTIVE LEAKAGE POWER	DE, VIVEK
10273627	6801463	150	10/17/2002	METHOD AND APPARATUS FOR LEAKAGE COMPENSATION WITH FULL VCC PRE-CHARGE	DE, VIVEK
10330652	Not Issued	20	12/27/2002	Multi-ported register files	DE, VIVEK
10748222	6903984	150	12/31/2003	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	DE, VIVEK
10748298	Not Issued	95	12/31/2003	TIMING CIRCUIT FOR SEPARATE POSITIVE AND NEGATIVE EDGE PLACEMENT IN A SWITCHING DC-DC CONVERTER	DE, VIVEK
10919672	Not Issued	25		Stepwise drivers for DC/DC converters	DE, VIVEK
10924482	Not Issued	41	08/23/2004	DC/DC converters using dynamically-adjusted variable-size switches	DE, VIVEK

10954464	Not Issued	30	09/30/2004	CPU power delivery system	DE, VIVEK
10987278	Not Issued	41	11/12/2004	Level shifter	DE, VIVEK
11066395	Not Issued	95	02/28/2005	FLOATING-BODY DRAM USING WRITE WORD LINE FOR INCREASED RETENTION TIME	DE, VIVEK
<u>11111060</u>	Not Issued	30	04/21/2005	Level shifter	DE, VIVEK
<u>11167978</u>	Not Issued	41	06/27/2005	Voltage regulation using digital voltage control	DE, VIVEK
11170559	Not Issued	30	06/28/2005	Low-voltage, buffered bandgap reference with selectable output voltage	DE, VIVEK
11173065	Not Issued	30	06/30/2005	Multiphase transformer for a multiphase DC-DC converter	DE, VIVEK
11173760	Not Issued	20	06/30/2005	DC-DC converter switching transistor current measurement technique	DE, VIVEK
11321100	Not Issued	19	01/01/0001	Reliability degradation compensation using body bias	DE, VIVEK
11323369	Not Issued	19	12/29/2005	Statistical circuit design with carbon nanotubes	DE, VIVEK
11323675	Not Issued	19	12/30/2005	Error-detection flip-flop	DE, VIVEK
11324628	Not Issued	19	01/03/2006	Bidirectional body bias regulation	DE, VIVEK
09218723	6154045	150	12/22/1998	METHOD AND APPARATUS FOR REDUCING SIGNAL TRANSMISSION DELAY USING SKEWED GATES	DE, VIVEK K
09470275	6518833	150	12/22/1999	LOW VOLTAGE PVT INSENSITIVE MOSFET BASED VOLTAGE REFERENCE CIRCUIT	DE, VIVEK K.
09505212	Not Issued	161	02/16/2000	Forward body biased transistors with reduced temperature	DE, VIVEK K.
09527344	6492837	150	03/17/2000	DOMINO LOGIC WITH OUTPUT PREDISCHARGE	DE, VIVEK K.
09537971	6359802	150	03/28/2000	One-transistor and one-capacitor dram cell for logic process technology	DE, VIVEK K.
09540230	Not	161	03/31/2000	Footless domino gate	DE, VIVEK K.

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<u>09607495</u>	6518796	150	06/30/2000	DYNAMIC CMOS CIRCUITS WITH INDIVIDUALLY ADJUSTABLE NOISE IMMUNITY	DE, VIVEK K.
09608314	6429711	150	06/30/2000	STACK-BASED IMPULSE FLIP- FLOP WITH STACK NODE PRE-CHARGE AND STACK NODE PRE-DISCHARGE	DE, VIVEK K.
09608457	6552887	150	06/29/2000	VOLTAGE DEPENDENT CAPACITOR CONFIGURATION FOR HIGHER SOFT ERROR RATE TOLERANCE	DE, VIVEK K.
09672689	6683467	150	09/29/2000	METHOD AND APPARATUS FOR PROVIDING ROTATIONAL BURN-IN STRESS TESTING	DE, VIVEK K.
09672695	6459293	150	09/29/2000	MULTIPLE PARAMETER TESTING WITH IMPROVED SENSITIVITY	DE, VIVEK K.
09672696	6632686	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	DE, VIVEK K.
09675579	6519176	150	09/29/2000	DUAL THRESHOLD SRAM CELL FOR SINGLE-ENDED SENSING	DE, VIVEK K.
09677698	6849909	150		METHOD AND APPARATUS FOR WEAK INVERSION MODE MOS DECOUPLING CAPACITOR	DE, VIVEK K.
09690687	6421269	150	10/17/2000	LOW-LEAKAGE MOS PLANAR CAPACITORS FOR USE WITHIN DRAM STORAGE CELLS	DE, VIVEK K.
09707528	6744301	150	11/07/2000	SYSTEM USING BODY- BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALITIES AND NOISE	DE, VIVEK K.
09727025	Not Issued	161	11/30/2000	Reference voltage translation circuit	DE, VIVEK K.
09727173		150	11/30/2000	Current reference	DE, VIVEK K.

<u>09727176</u>	6433624	150	11/30/2000	THRESHOLD VOLTAGE GENERATION CIRCUIT	DE, VIVEK K.
09731515	6486706	150	12/06/2000	DOMINO LOGIC WITH LOW- THRESHOLD NMOS PULL-UP	DE, VIVEK K.
09740104	6351156	150	12/18/2000	Noise reduction circuit	DE, VIVEK K.
09820067	6429726	150	03/27/2001	ROBUST FORWARD BODY BIAS GENERATION CIRCUIT WITH DIGITAL TRIMMING FOR DC POWER SUPPLY VARIATION	DE, VIVEK K.
09820579	6608513	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	DE, VIVEK K.
09821531	6469572	150	03/28/2001	FORWARD BODY BIAS GENERATION CIRCUITS BASED ON DIODE CLAMPS	DE, VIVEK K.
09823575	6608786	150	03/30/2001	APPARATUS AND METHOD FOR A MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME	DE, VIVEK K.
09823633	6496040	150	03/30/2001	TRADING OFF GATE DELAY VERSUS LEAKAGE CURRENT USING DEVICE STACK EFFECT	DE, VIVEK K.
09846514	Not Issued	161	04/30/2001	CMOS bus pulsing	DE, VIVEK K.
09846604	6515513	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	DE, VIVEK K.
09855910	6445216	150	05/14/2001	SENSE AMPLIFIER HAVING REDUCED VT MISMATCH IN INPUT MATCHED DIFFERENTIAL PAIR	DE, VIVEK K.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
10956195	Not Issued	93		SRAM CELL POWER REDUCTION CIRCUIT	TSCHANZ, JAMES
11323675	Not Issued	19	12/30/2005	Error-detection flip-flop	TSCHANZ, JAMES
09608314	6429711	150	06/30/2000	STACK-BASED IMPULSE FLIP-FLOP WITH STACK NODE PRE-CHARGE AND STACK NODE PRE- DISCHARGE	TSCHANZ, JAMES W.
09672696	6632686	150	09/29/2000	SILICON ON INSULATOR DEVICE DESIGN HAVING IMPROVED FLOATING BODY EFFECT	TSCHANZ, JAMES W.
09707528	6744301	150	11/07/2000	SYSTEM USING BODY- BIASED SLEEP TRANSISTORS TO REDUCE LEAKAGE POWER WHILE MINIMIZING PERFORMANCE PENALITIES AND NOISE	TSCHANZ, JAMES W.
09820579	6608513	150	03/28/2001	FLIP-FLOP CIRCUIT HAVING DUAL-EDGE TRIGGERED PULSE GENERATOR	TSCHANZ, JAMES W.
09846514	Not Issued	161	04/30/2001	CMOS bus pulsing	TSCHANZ, JAMES W.
09846604	6515513	150	04/30/2001	REDUCING LEAKAGE CURRENTS IN INTEGRATED CIRCUITS	TSCHANZ, JAMES W.
09894465	6763484	150	06/28/2001	BODY BIAS USING SCAN CHAINS	TSCHANZ, JAMES W.
10010046	6642765	150	12/06/2001	TRANSMISSION-GATE BASED FLIP-FLOP	TSCHANZ, JAMES W.
10267951	6784722	150	10/09/2002	WIDE-RANGE LOCAL BIAS GENERATOR FOR BODY	TSCHANZ, JAMES W.

				BIAS GRID	
10328573	Not Issued	71	12/23/2002	Method and apparatus for reducing power consumption through dynamic control of supply voltage and body bias	TSCHANZ, JAMES W.
10330544	6806739	150	12/30/2002	TIME-BORROWING N-ONLY CLOCKED CYCLE LATCH	TSCHANZ, JAMES W.
10334410	6784688	150	12/30/2002	SKEWED REPEATER BUS	TSCHANZ, JAMES W.
10334746	Not Issued	30		Method and apparatus for bus repeater tapering	TSCHANZ, JAMES W.
10673283	Not Issued	161		Local bias generator for adaptive forward body bias	TSCHANZ, JAMES W.
10703562	Not Issued	41	11/10/2003	Method and apparatus for power consumption reduction	TSCHANZ, JAMES W.
10738216	Not Issued	95	12/18/2003	METHOD AND APPARATUS TO CLAMP SRAM SUPPLY VOLTAGE	TSCHANZ, JAMES W.
10745029	7015741	150	12/23/2003	ADAPTIVE BODY BIAS FOR CLOCK SKEW COMPENSATION	TSCHANZ, JAMES W.
10746759	Not Issued	93	12/23/2003	IC DESIGN PROCESS INCLUDING AUTOMATED REMOVAL OF BODY CONTACTS FROM MOSFET DEVICES	TSCHANZ, JAMES W.
10747805	Not Issued	61	12/29/2003	Method and apparatus for applying body bias to integrated circuit die	TSCHANZ, JAMES W.
10792262	6917237	150	03/02/2004	TEMPERATURE DEPENDENT REGULATION OF THRESHOLD VOLTAGE	TSCHANZ, JAMES W.
10812894	Not Issued	71	03/31/2004	SRAM device having forward body bias control	TSCHANZ, JAMES W.
10813084	6992603	150	03/31/2004	SINGLE-STAGE AND MULTI- STAGE LOW POWER INTERCONNECT ARCHITECTURES	TSCHANZ, JAMES W.
10873243	6970018	150	06/23/2004	CLOCKED CYCLE LATCH CIRCUIT	TSCHANZ, JAMES W.
10879486	Not Issued	20	06/30/2004	Method, apparatus and system of adjusting one or more performance-related parameters of a processor	TSCHANZ, JAMES W.
10880988	Not	71	06/30/2004	Interconnect structure in	TSCHANZ, JAMES

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10947765	Not Issued	30	09/23/2004	Majority voter apparatus, systems, and methods	TSCHANZ, JAMES W.
10947869	Not Issued	41	09/23/2004	Gating for dual edge-triggered clocking	TSCHANZ, JAMES W.
10953199	Not Issued	41	09/28/2004	Frequency management apparatus, systems, and methods	TSCHANZ, JAMES W.
10953865	Not Issued	30	09/30/2004	System and method for applying within-die adaptive body bias	TSCHANZ, JAMES W.
10954256	Not Issued	30	09/29/2004	Control circuitry in stacked silicon	TSCHANZ, JAMES W.
10955383	Not Issued	20	09/30/2004	Power management integrated circuit	TSCHANZ, JAMES W.
10982266	Not Issued	30	11/03/2004	Processor apparatus with body bias circuitry to delay thermal throttling	TSCHANZ, JAMES W.
11018011	Not Issued	30	12/20/2004	Body biasing for dynamic circuit	TSCHANZ, JAMES W.
<u>11018016</u>	Not Issued	25	12/20/2004	Body biasing methods and circuits	TSCHANZ, JAMES W.
11038134	Not Issued	30	01/21/2005	Bias generator for body bias	TSCHANZ, JAMES W.
11038394	Not Issued	30	01/21/2005	Bias generator for body bias	TSCHANZ, JAMES W.
11053788	Not Issued	30	02/09/2005	Majority voter circuit design	TSCHANZ, JAMES W.
11059174	Not Issued	20	02/16/2005	Representative majority voter for bus invert coding	TSCHANZ, JAMES W.
11094574	Not Issued	25	03/31/2005	Method and apparatus to adjust die frequency	TSCHANZ, JAMES W.
11134450	Not Issued	30	05/23/2005	Reducing power consumption in integrated circuits	TSCHANZ, JAMES W.
11295400	Not Issued	20	12/06/2005	Component reliability budgeting system	TSCHANZ, JAMES W.
11314236	Not Issued	20	12/22/2005	Single-stage and multi-stage low power interconnect architectures	TSCHANZ, JAMES W.
11320789	Not Issued	20	12/30/2005	Method and apparatus to clamp- SRAM supply voltage	TSCHANZ, JAMES W.
11321100	Not Issued	19	01/01/0001	Reliability degradation compensation using body bias	TSCHANZ, JAMES W.
11324628	Not Issued	19	01/03/2006	Bidirectional body bias regulation	TSCHANZ, JAMES W.

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